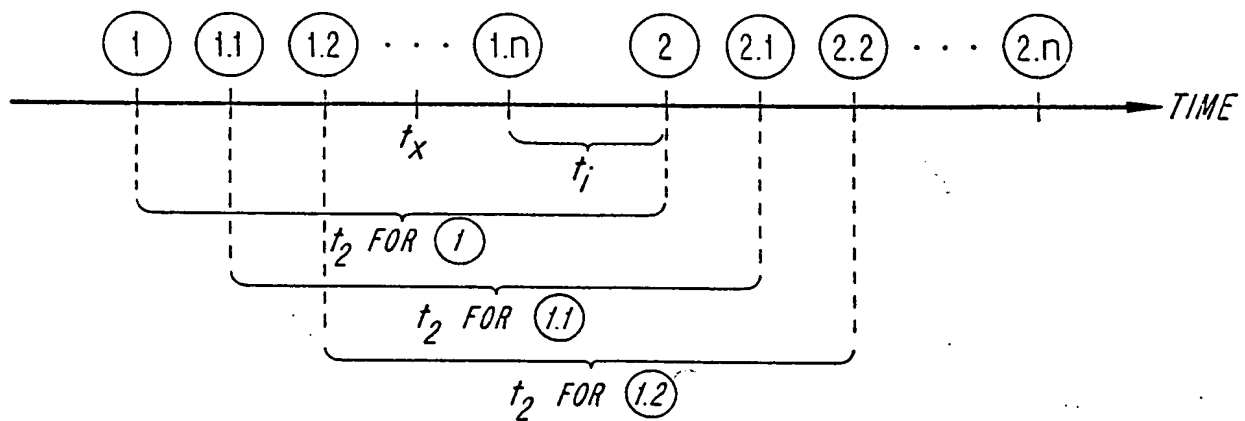
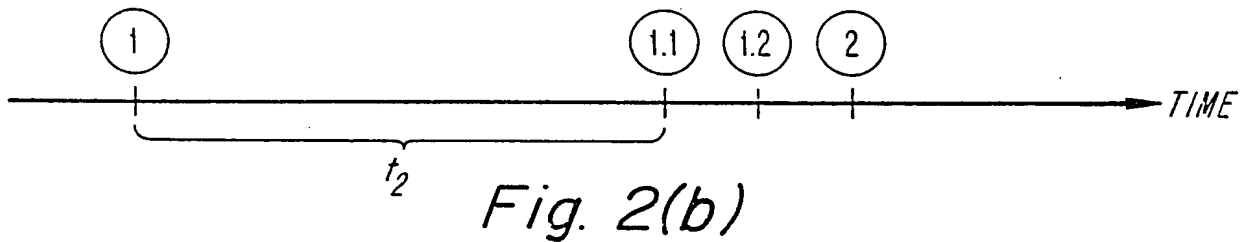
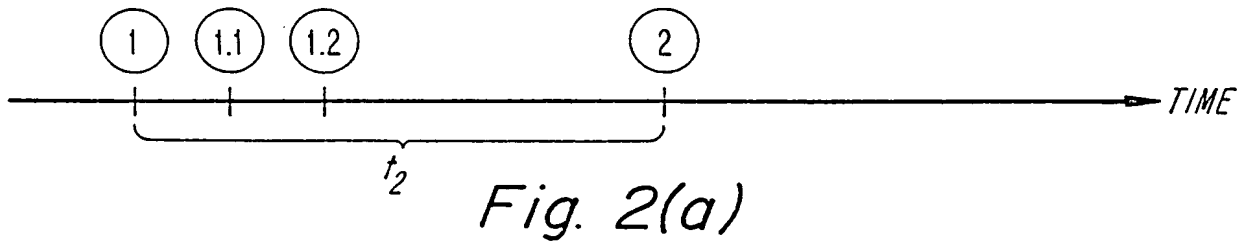
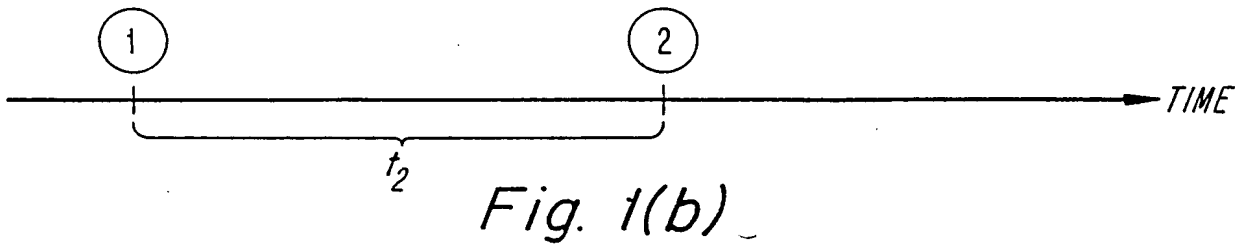
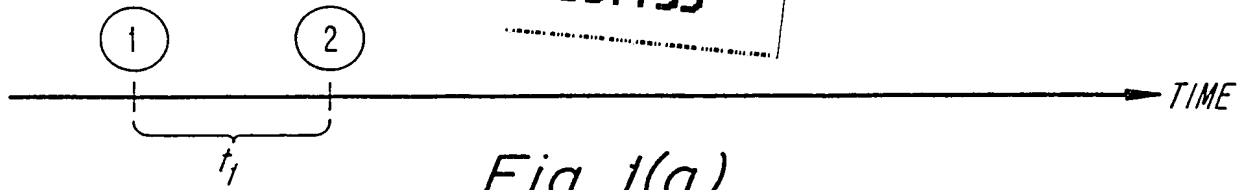


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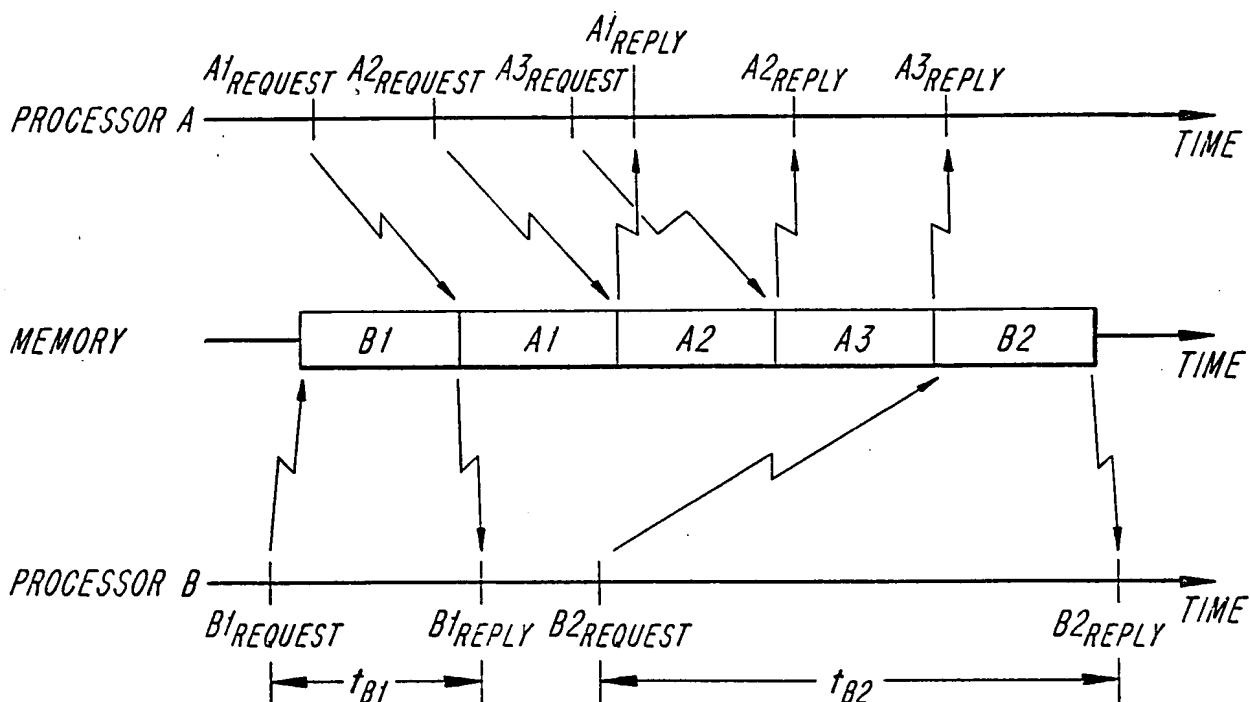


Fig. 3(a)

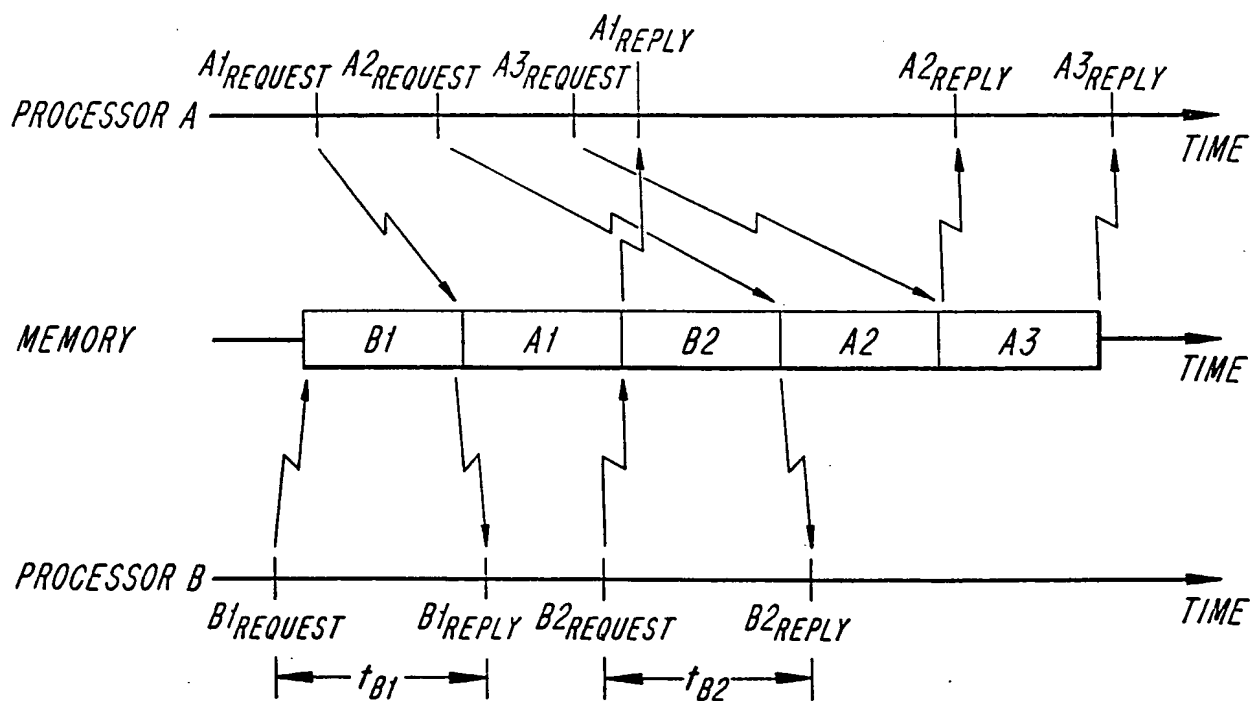


Fig. 3(b)

The diagram illustrates a system architecture for managing data flow between multiple processors and devices. On the left, a **CACHE** (20) is connected to a central horizontal bus. Below the bus are **PROCESSOR 0** (30<sub>0</sub>), **PROCESSOR 1** (30<sub>1</sub>), and **PROCESSOR m** (30<sub>m</sub>). Above the bus is a **NON-BLOCKING LOAD BUFFER** (10). To the right of the bus are **DEVICE 0** (50<sub>0</sub>), **DEVICE 1** (50<sub>1</sub>), and **DEVICE n** (50<sub>n</sub>). Each device has a **READY** output line. The bus is labeled with reference numerals 40, 41, and 42. Arrows indicate the direction of data flow: from processors to the bus, from the bus to the non-blocking load buffer, and from the non-blocking load buffer to the devices. Ellipses (...) indicate multiple intermediate processors and devices.

APPROVED	C.G. FIG. 3(6)	
	CLASS	SUBCLASS
BY	395	872
DRAFTSMAN		

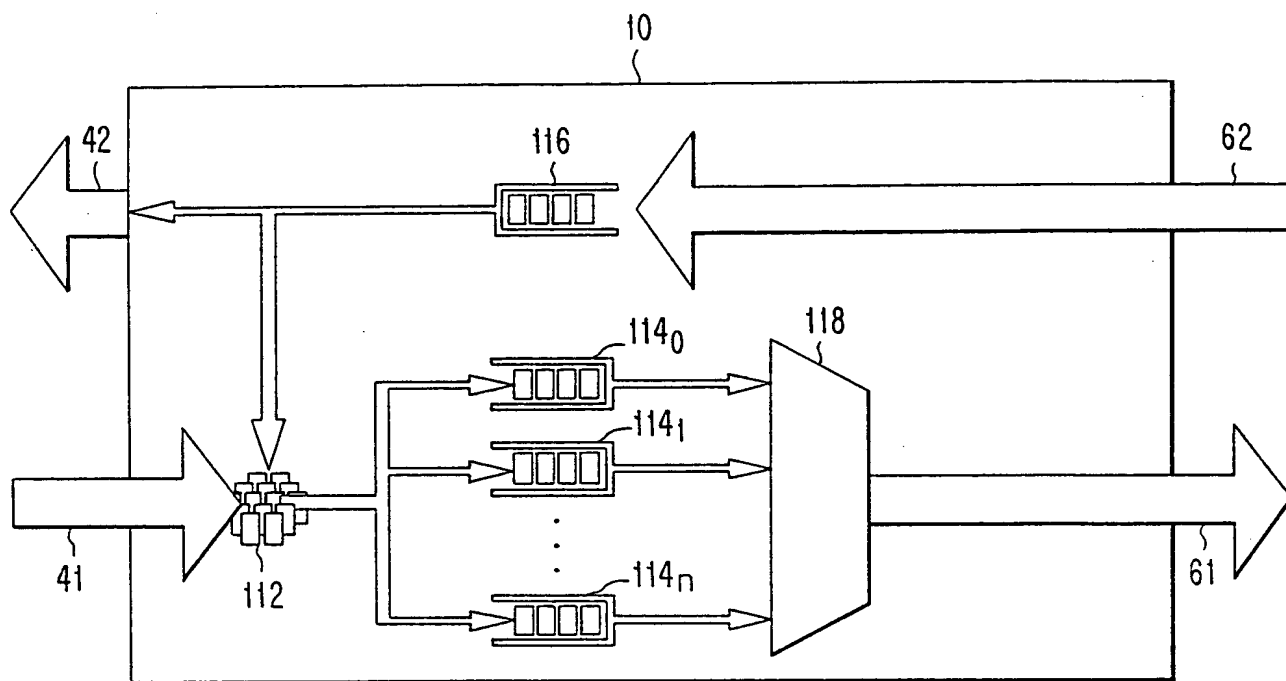


Fig. 5

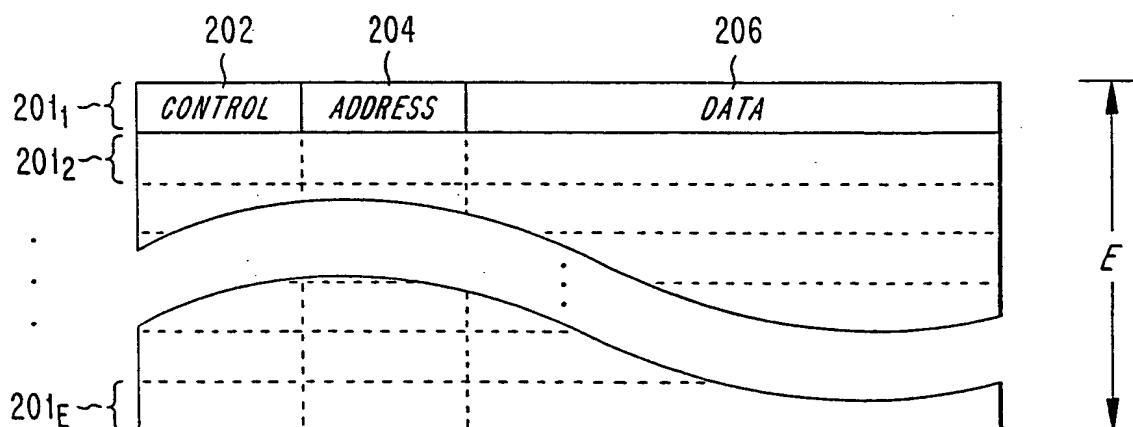


Fig. 6

200

APPROVED	O.G. FIG. 3(2)
BY	CLASS
DRAFTSMAN	395
	872

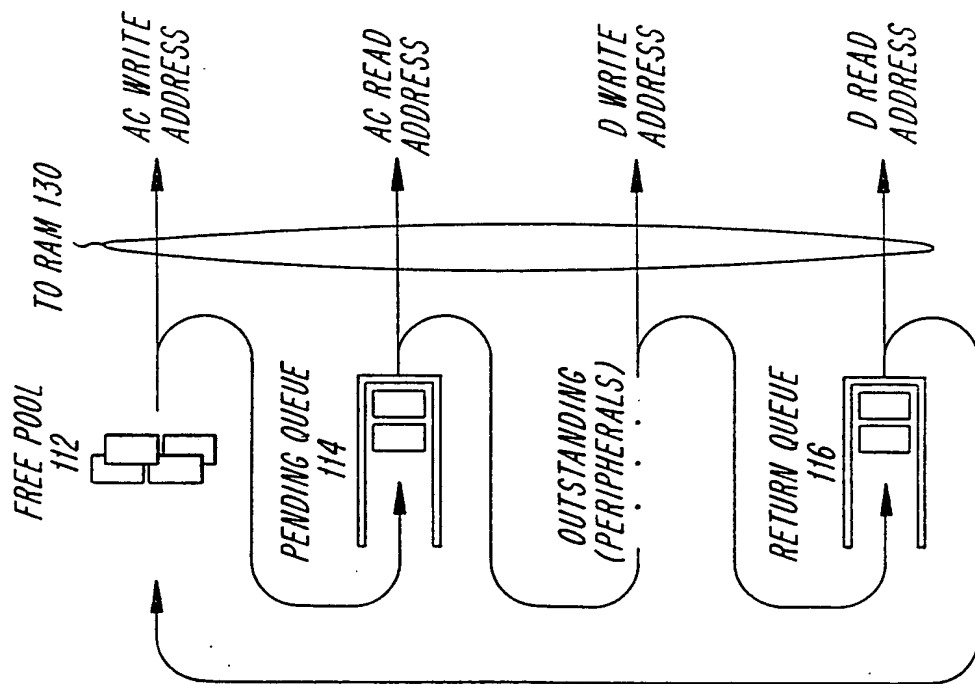


Fig. 7(a)

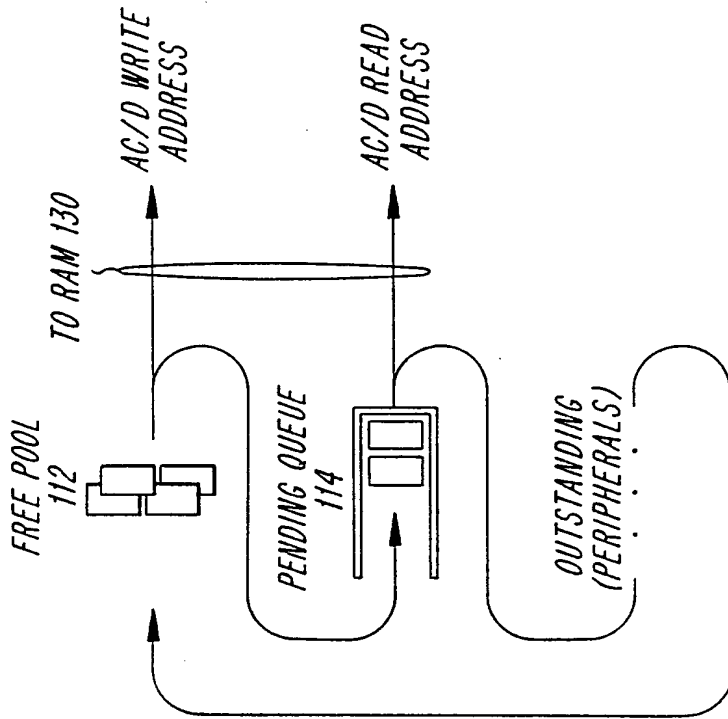


Fig. 7(b)

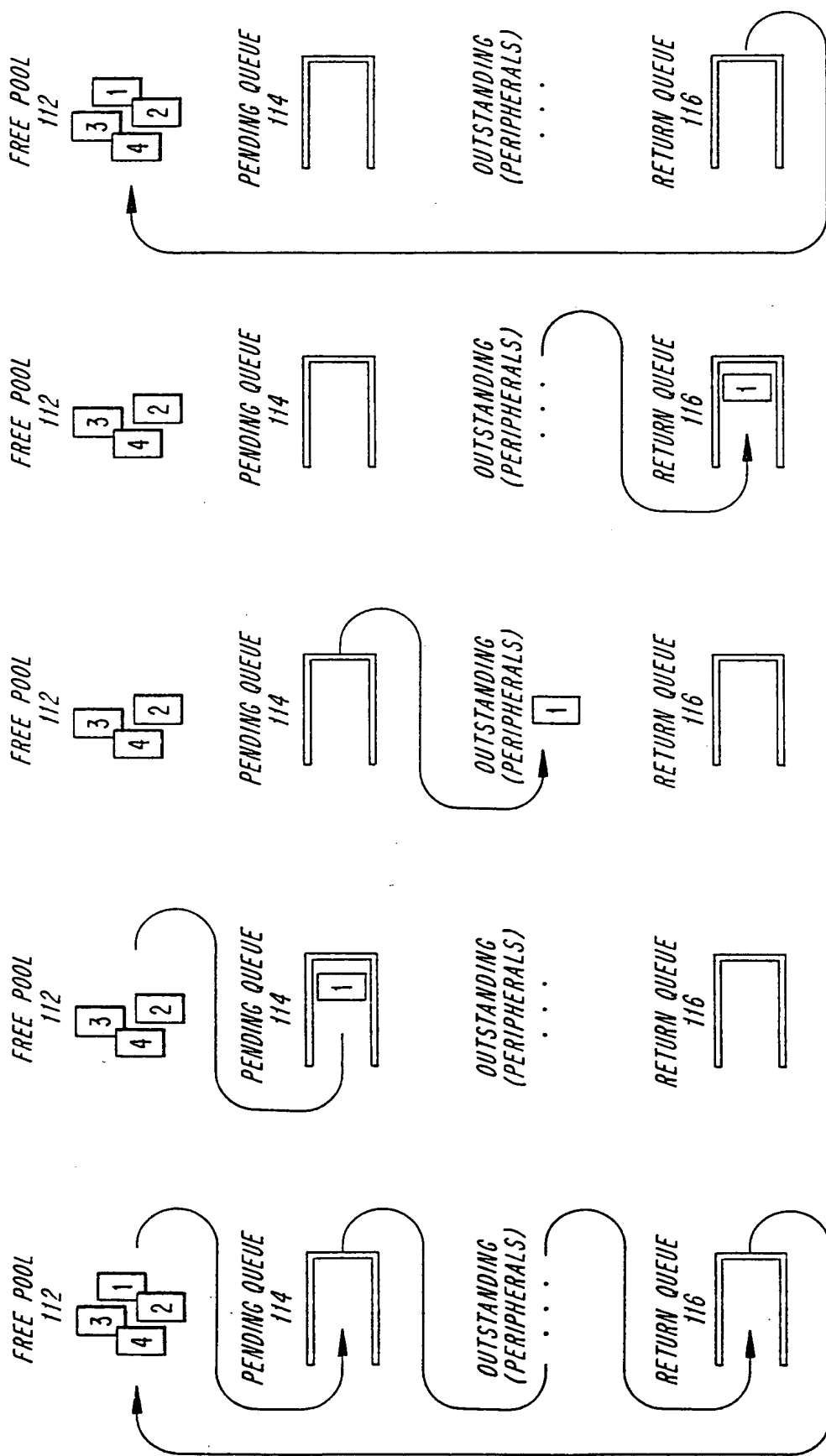


Fig. 7(g)

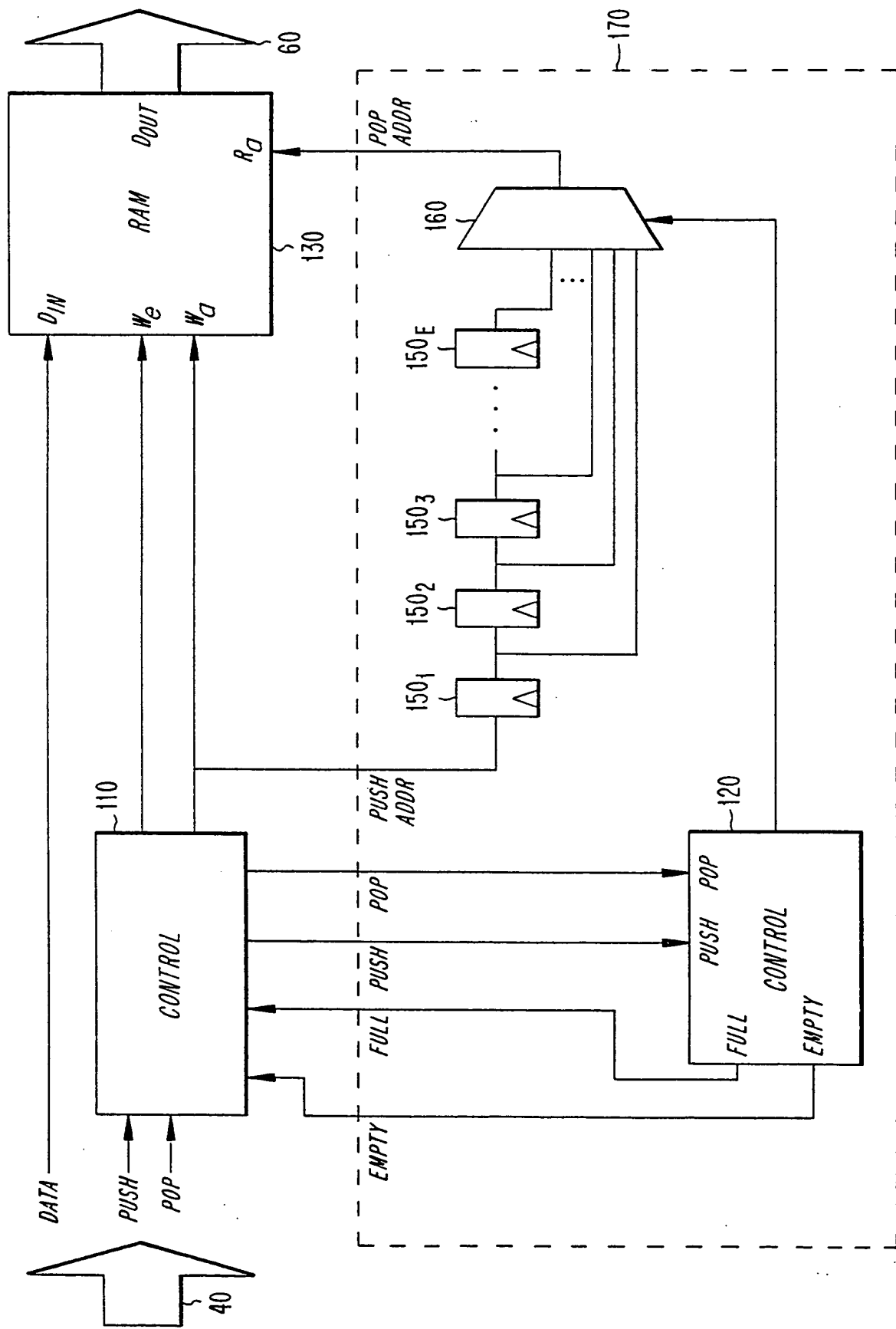


Fig. 8

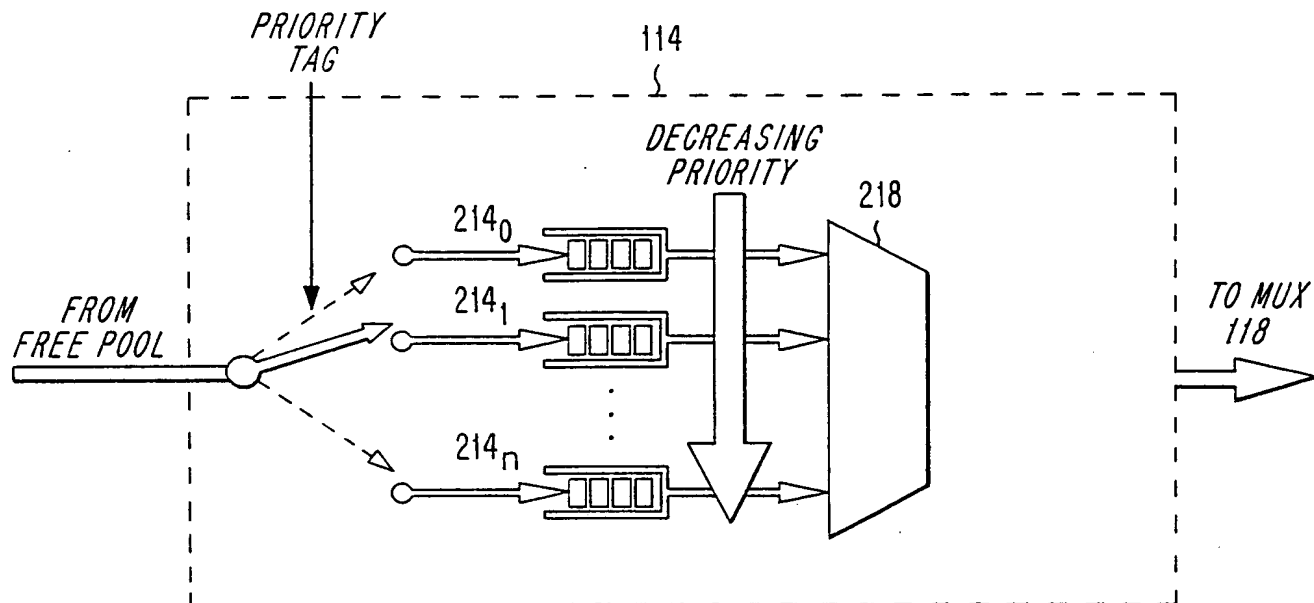


Fig. 9(a)

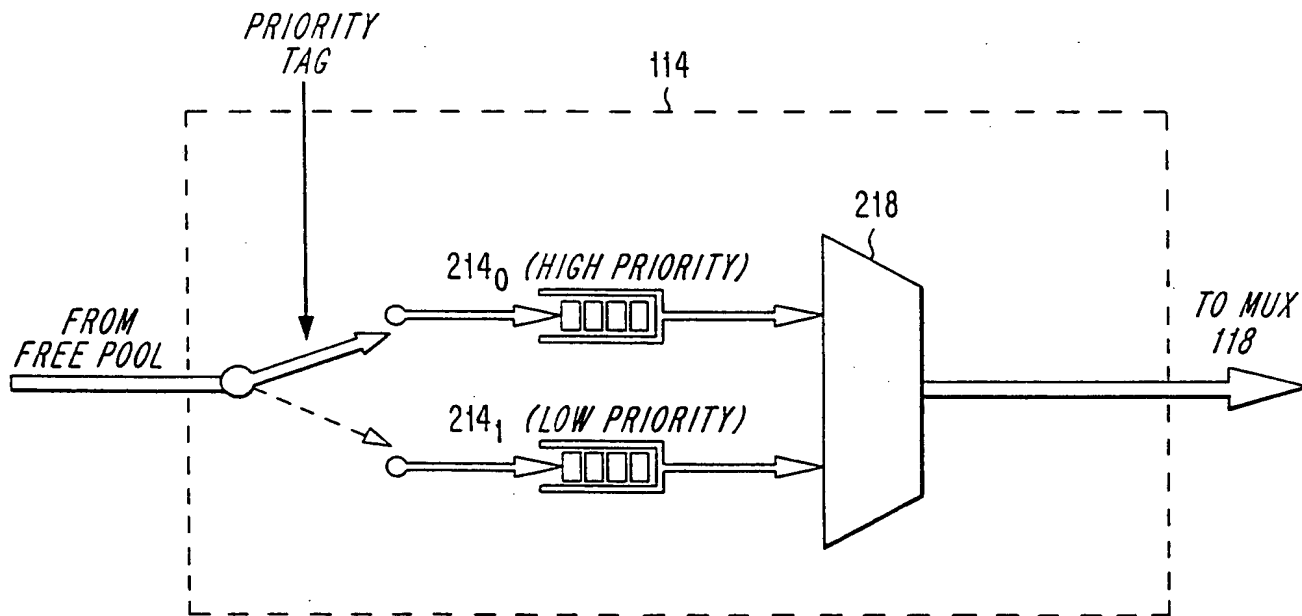


Fig. 9(b)

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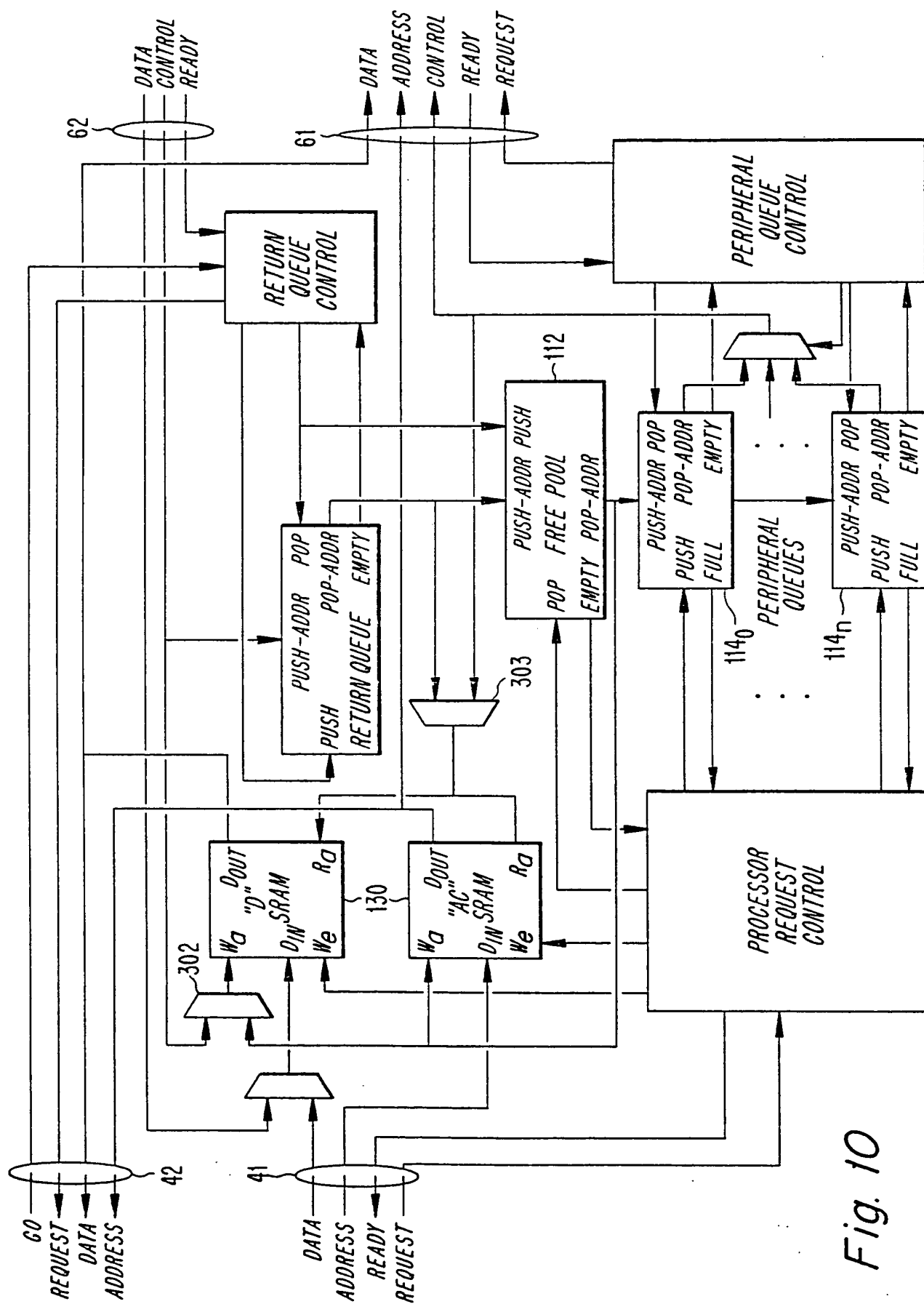


Fig. 10

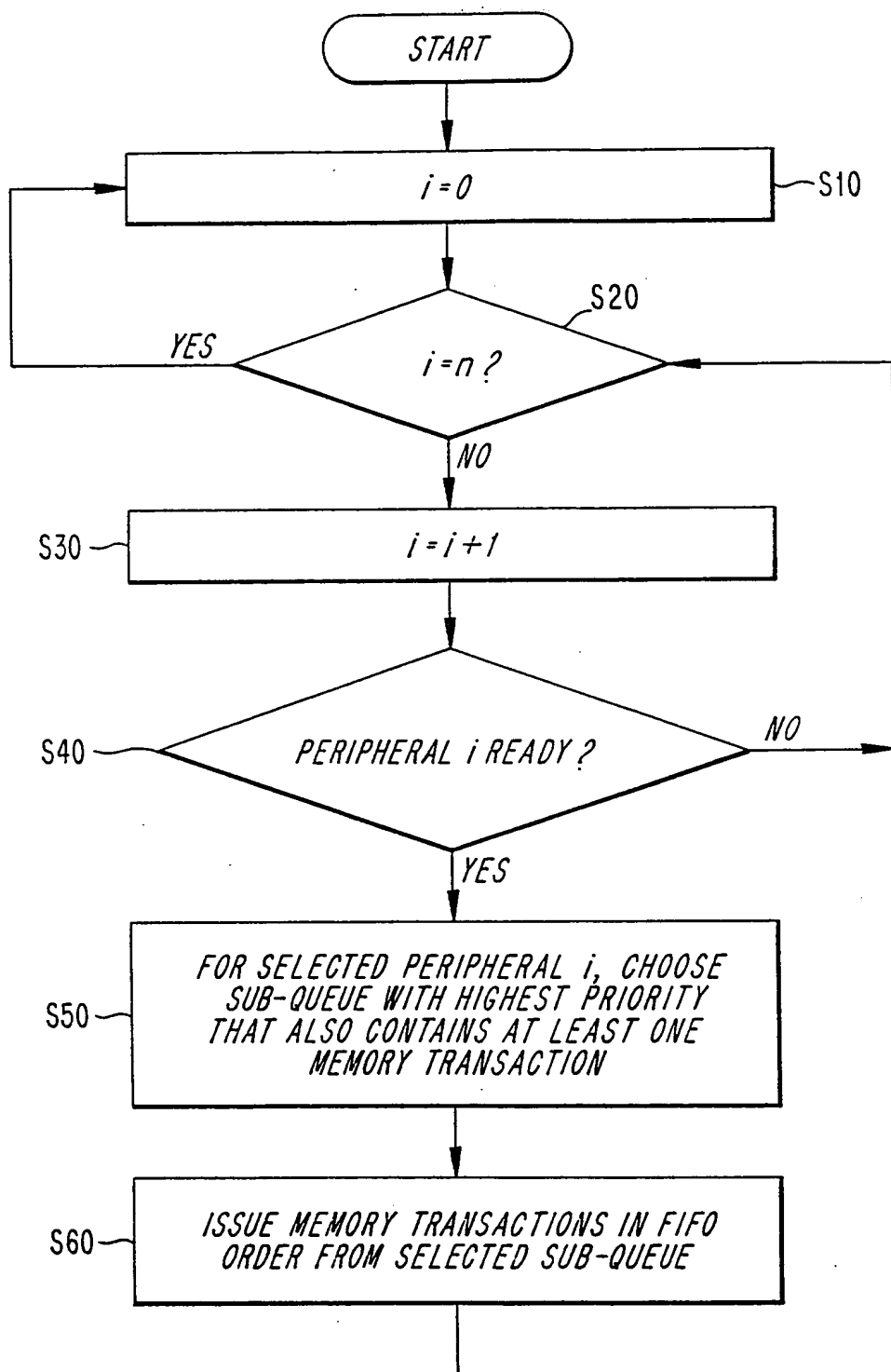


Fig. 11